Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 2-72.

Listing of Claims:

1. (Original) A memory device data path, comprising:

a storage device storing N bits of data;

a first bus having N/2 bits coupled to the storage device;

a second bus having N/2 bits coupled to the storage device;

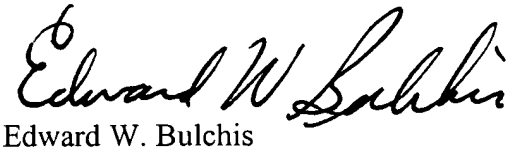
a first set of N/2M parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, the parallel-to-serial converters in the first set being operable in a first operating mode to receive from the storage device through the first bus 2 sets of parallel data each containing M bits and apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of N/2M parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, the parallel-to-serial converters in the second set being operable in the first operating mode to receive from the storage device through the second bus 2 sets of parallel data each containing M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, the parallel-to-serial converters in the second set being operable in a second operating mode to receive from the storage device through the first and second buses a set of parallel data containing 2M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

Claims 2-72 (Cancelled).

Respectfully submitted,

DORSEY & WHITNEY LLP



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